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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,876	02/26/2002	Brian James Knight	56162.000304	6208

21967 7590 09/08/2004

HUNTON & WILLIAMS LLP
INTELLECTUAL PROPERTY DEPARTMENT
1900 K STREET, N.W.
SUITE 1200
WASHINGTON, DC 20006-1109

EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,876	KNIGHT, BRIAN JAMES	
	Examiner	Art Unit	
	Henry W.H. Tsai	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/26/02* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: at page 5, the table should be labeled as "Table 1".

Appropriate correction is required.

Drawings

2. The drawings are objected to because

in Fig. 1, the figure only comprises blocks and lines. For better illustrative purpose, each block should contain a device name represented.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, last line, it is not clear which one "the register" is referred to since there are two registers, a register and a PC register, mentioned in line 8. Similar problems exist in claims 9 and 17.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-7, 9-15, and 17-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Schan, Jr. et al. (U.S. Patent No. 5,003,466), herein referred to as Schan, Jr. et al.'855.

Referring to claim 1, Schan, Jr. et al.'855 discloses as claimed a method for separating exception vectors (see Col. 6, lines 53-63 regarding the separate tables for non-normal exceptions and interrupts) in a data processing system having at least two processors (processors 100, 100 inside 12 and 25, see Fig. 1), comprising the steps of: receiving an exception request (this is deemed inherent to occur when an exception is encountered in the Schan, Jr. et al.'855's system) into one of the at least two processors; entering, in the processor receiving the exception request, an exception mode (this is the situation when the process switch mechanism is used by interrupts and non-normal exceptions, see Col. 6, lines 12-14) relating to the received exception request; calling an instruction located at a portion of an exception vector table (see the vector table 201 in Fig. 2, see also Col. 6, lines 51-

52, and 56-58, regarding the exception vector table comprising the starting address or control block pointers to the instruction for the system call) associated with the type of exception request received, wherein the instruction causes the moving of a register into a program counter register (see Fig. 2, the register 214 storing program counter) of the processor receiving the exception request; and executing a processor-specific exception handling routine (see Col. 6, lines 50-59, regarding the handling routine tables containing the processor status words and program counter values for the a group of functions; and for non-normal exceptions, the operating system provides an exception-vector table which contains the process control block pointers of the non-normal exception handler processes) relating to the received exception request, the address of the processor-specific exception handling routine being maintained in the register (as set forth above, the vector table 201 in Fig. 2, see also Col. 6, lines 51-52, and 56-58, regarding the exception vector table comprising the starting address or control block pointers to the instruction for the system call). Note claims 9 and claim 17 each recite the corresponding limitations which are disclosed or taught by Schan, Jr. et al.'855 as set forth above in claim 1.

As to claims 2, 10, and 18, Schan, Jr. et al.'855 also discloses the step of entering an exception mode, further comprises the step of replacing a normal register (the registers in main memory 13, see Fig. 1) in the processor receiving the exception request with a processor-specific exception mode banked register (the register in the vector table 201 for exception processes, see Fig. 2).

As to claims 3, 11, and 19, Schan, Jr. et al.'855 also discloses the register (the register 214 comprising INTM PC, see Fig. 2) moved into the program counter is the processor-specific exception mode banked register (the register in the vector table 201 for exception processes, see Fig. 2).

As to claims 4, 12, and 20, Schan, Jr. et al.'855 also discloses the step of initializing (see Col. 6, lines 59-62, regarding the OS proving the initial process control block pointers in the interrupt vector table) the processor-specific exception mode banked register to contain the address of the exception handling routine.

As to claims 5, 13, and 21, Schan, Jr. et al.'855 also discloses the exception request is an interrupt request (IRQ) (this is the situation when an interrupt occurs, see Col. 6, lines 59-63, and the interrupt vector table such as 201 in Fig. 2 is used).

As to claims 6, 14, and 22, Schan, Jr. et al.'855 also discloses processor-specific exception mode banked register is a processor-specific IRQ mode banked register (as set forth above, this is the situation when an interrupt occurs, see Col. 6, lines 59-63, and the interrupt vector table such as 201 in Fig. 2 is used).

As to claims 7, 15, and 23, Schan, Jr. et al.'855 also discloses the instruction located at a portion of an exception vector table associated with the type of exception request received, is an instruction taking the form "move pc, r13" (note this is deemed to be inherent since the values in registers 213 or 214 are essentially to be moved to the PC of the Schan, Jr. et al.'855's system), indicating that the contents of the r13 register are to be moved into the program counter register (the register 214 comprising INTM PC, see Fig. 2).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section

102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 8, 16, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schan, Jr. et al.'855 in view of Browning et al. (U.S. Patent No. 6,732,138), hereafter referred to as Browning et al.'138.

Schan, Jr. et al.'855 discloses the claimed invention except for explicitly showing that it comprises: the at least two processor are reduced instruction set computing (RISC) processors (claims 8, 16, and 24).

Browning et al.'138 discloses a system (12 see Fig. 2) comprising the at least two processor (30, 30 in the IBM RISC System/6000, see Fig. 2, and see also Col. 4, lines 35-38) are reduced instruction set computing (RISC) processors.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Schan, Jr. et al.'855's system to comprise the at least two processor are reduced instruction set computing (RISC) processors, as taught

by Browning et al.'138, in order to enable executing a thread within one of a number of concurrent multithreaded processes (see Col. 4, lines 38-45) to increase the total performance for the Schan, Jr. et al.'855's system.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mohammed et al.'838 also discloses Coordination and synchronization of an asymmetric, single-chip, dual multiprocessor. Table A. 2 show a exception vector table comprising different type of exceptions. Hohensee et al.'452 discloses a method and a multiprocessor computer for execution of the method. A first CPU has a general register file, an instruction pipeline, and profile circuitry. A second CPU is configured to analyze the generated profile data, while the execution and profile data generation continue on the first CPU, and to control the execution of the program on the first CPU based at least in part on the analysis of the collected profile data.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

11. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number:** 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
September 2, 2004